REMARKS

This is intended as a full and complete response to the Office Action dated August 22, 2003, having a shortened statutory period for response set to expire on November 22, 2003 (the "Office Action"). Claim 14 has been canceled without prejudice. Claims 1, 4, 5-8, 10, and 15 have been amended. Accordingly, with the entry of this Amendment, claims 1-13, and 14-34 remain in the application.

In the Office Action, claims 1-4, 6-13, and 15-34 were rejected under 35 USC 102(b) as being anticipated by Pressly *et al.* (U.S. Pat. No. 5,889,788; "Pressly").

Claim 1 recites among other features, a method for performing a timing analysis for a core device to be embedded in a programmable logic device (PLD), comprising determining setup and hold timing information and delay timing information for a portion of the programmable logic device. In Pressly the IC contains two primary circuit portions, the customer specific logic 12 connected to the embedded core 14 via some test path cells (FIG.1, col. 6 lines 15-18 and 60-62). Pressly does not disclose nor suggest a core device embedded in a PLD. Hence for at least this reason alone claim 1 should be allowable.

Additionally, in the Office Action, with respect to claims 9, 15-18, 25, 26, 33, and 34, it is stated that Pressly discloses "...a field programmable logic device..." citing column 6 of Pressly. At column 6, from line 21 to line 34, Pressly provides a general disclosure regarding an integrated circuit. However, nothing in Pressly describes or shows that the integrated circuit has programmable circuitry as in a programmable logic device, or more particularly a field programmable gate array. Pressly's examples of customer specified logic are application specific logic circuits ("ASICs"). In fact, signal nomenclature in Pressly indicates that an ASIC is used (*see generally,* Pressly at col. 9, lines 12-15 regarding a "test_core/asicbar" signal). Furthermore, a

need for special circuits for testing (*see*, Pressly at col. 12, lines 5-11) at least suggests that dedicated circuitry, different from programmable circuitry as in a programmable logic device, is used. Accordingly, Applicant respectfully disagrees with the characterization in the Office Action that Pressly discloses a "field programmable logic device" as claimed in claims 9 and 18, or for that matter a programmable logic device as claimed in claims 1 and 17.

Thus for at least the above reasons claim 1 should be allowable. Claims 2-9 being dependent upon claim should be allowable for at least the reasons claim 1 is allowable.

In the Office Action, it is stated that claims 5 and 14 would be allowable if rewritten. With respect to the reason for allowing claims 5 and 14, the Office Action states: "The primary reason is the inclusion of the step of feeding back the circuitry values and modifications of the portion of the host integrated circuit for re-determination of at least on of the setup and hold timing information and the delay timing information for the portion of the host integrated circuit, in a method for performing a timing analysis for a core device to be embedded in a host integrated circuit."

Claim 10 has been amended to recite in relevant part: "…feeding back the circuitry values and modifications of the portion of the host integrated circuit for re-determination of at least one of the clock-to-output timing information and the delay timing information for the portion of the host integrated circuit." Hence, it is respectfully submitted that the feed back steps recited in amended claim 10 are not shown or described in Pressly and claim 10 should be allowable.

Claims 11-13 and 15-18 being dependent upon claim 10 should be allowable for at least the reasons claim 10 is allowable.

In addition in the Office Action, with respect to claim 3, 4, 12, and 13, it is stated that Pressly discloses "…determining circuitry values in response to modification…" citing columns 19-21 of Pressly. However, Applicant could find no such disclosure in Pressly. Accordingly, Applicant respectfully

disagrees with the characterization in the Office Action that Pressly discloses "determining circuitry values in response to modification".

Claims 19 and 27 recite among other features, inputting the delay times, the setup and hold times and the clock-to-output times to a spreadsheet; and determining path times from the spreadsheet. Pressly does not disclose nor suggest such features. Hence for at least this reason alone claims 19 and 27 should be allowable.

Claims 20-26 and 28-34 being dependent upon claims 19 and 27, respectively, should be allowable for at least the reasons claims 19 and 27 are allowable.

CONCLUSION

All claims should be now be in condition for allowance and a Notice of Allowance is respectfully requested.

If there are any questions, the applicants' attorney can be reached at Tel: 408-879-6149 (Pacific Standard Time).

Respectfully submitted,

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I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450, on November 24, 2003.

Pat Slaback
Name

Signature